REMARKS/ARGUMENTS

Claims 1-20 remain pending in this application and stand rejected. Claims 1-3, 8-9, and 20 stand rejected under 35 U.S.C. § 101 as being non-statutory for failing to produce any real world tangible result. Claims 1-3, 8-9 and 18 further stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns el al., U.S. Patent 6,819,679, (hereinafter Kerns), Sakalian et al. (U.S. Patent No. 5,056,119, hereinafter Sakalian) in view of Koyama (U.S. Patent No. 6,047,04 hereinafter Koyama).

Claims 4-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns, Sakalian, Koyama, in view of Wright et al. (U.S. Patent No. 7,103,049, hereinafter Wright). Claim 19 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns, Sakalian, O'Conner, in view of Mao et al. (U.S. Patent No. 7,151,773, hereinafter Mao). Claim 20 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns, Sakalian, O'Conner, in view of Taborek, Sr. et al. (US 7,020, 729, hereinafter Taborek). Claims 10, 13-16, and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Taborek further in view of Wright. Claims 11-12 stand rejected under Taborek, Wright, and further in view of Swoboda et al. (US Patent No. 6,085,336, hereinafter Swoboda). Applicants respectfully traverse the above rejections for at least the reasons that follow.

Claim 1 is amended to recite, in part, "synchronizing the serial stream of incoming data in accordance with the determined synchronization pattern." In view of this amendment, reconsideration of the rejections under 35 U.S.C. § 101 is respectfully requested.

Applicant submits that claim 1 is patentable over the combinations of Kerns, Sakalian and Koyama for at least the reasons cited below. As pointed out correctly by the Examiner, Kerns fails to teach "selecting a first position from a first plurality of possible positions; if the first selected position is not correct, selecting a second position from a second plurality of possible positions, wherein each of the second plurality of possible positions comprises each of the first plurality of possible positions shifted by one position unit, and determining the position of the synchronization pattern in the serial stream of incoming data using the selected second position.."

The Examiner's asserts that Sakalian teaches "selecting a first position from a plurality of positions and if the selected position is not correct, selecting a second position from a second plurality of possible positions" (column 1, line 16-column 2, line 7) and (column 1, lines 16-25). As best understood, Sakalian relies on bit positions within a stream of data to determine synchronization. In column 1, lines 41-67, and column 2, lines 1-8, cited by the Examiner, Sakalian states:

"In other words, the present circuit operates on the principle that if five consecutively received bits in the selected framing bit position follow a predetermined pattern that the correct data bit position has been established. If three out of five later received bits are detected as being incorrect, (after synchronization has been established) it may be assumed that the problem is not in the selection of the wrong framing bit position, but rather in the transmission medium. If any further data bits are received in the data bit position previously selected as the framing bit position, and these bits are received with incorrect values as compared to the predetermined pattern, it may be safely assumed that a new transmission medium needs to be established and resynchronization needs to be commenced from an initial set of values. On the other hand, if the next several framing bit positions provide the correct logic values, it may be correctly assumed that the interference problem causing the incorrect detection of logic values of data bits was a momentary occurrence and that in spite of the interference, synchronization with the transmitter has not actually been lost and thus there is no need to return to the very time consuming process of reestablishing synchronization from "scratch". As will be realized, under the worst possible conditions where there are many logic zero bit positions between framing bits, and where the framing bits alternate in logic value, it could take a large amount of time equal to the time of transmission of many data frames to establish the correct data bit position for the framing bit. Thus, it is very advantageous to temporarily return to the confirmation mode where possible, and reestablish that the correct bit position was selected and is still valid rather than returning to the selection mode to reestablish synchronization."

The Examiner also asserts that Koyama teaches "wherein each of the second plurality of positions shifted by one position unit wherein the selected position is used to determine the position of the synchronization pattern in the serial stream of incoming data. Below are lines 11-54, of column 2 of Koyama, reproduced below for the Examiner's convenience:

"According to the present invention, the synchronizing device comprises: a shift register having a plurality of buffers each having a storage capacity of m bits for successively holding the second unit data forming the input data signal; a pattern data extracting portion for extracting L-bit-long data from the data held in the shift register in correspondence with first to K(≥1)th patterns in which the first unit data is sequentially assigned in the second data signal to obtain first to Kth extraction data; a first comparator portion for comparing each of the first to Kith extraction data with a synchronizing code as an indicator of a head word of the packet; a pattern selecting portion for selecting and outputting one of the first to Kth extraction data as an extraction signal; a state transition control portion for controlling the selecting operation of the pattern selecting portion depending on whether it is in a synchronous state or an asynchronous state; and a synchronization determining portion for determining whether it is in the synchronous state or the asynchronous state.

In this device, the state transition control portion comprises a mode shifting portion for causing the pattern selecting portion to cyclically and sequentially select the first to Kth extraction data so that continuous L-bit-unit data are sequentially extracted from the input data signal, and a mode changing portion for, only in the asynchronous state, every time the comparison in the first comparator portion shows that only a kth (1 ≤k.≤.K) extraction data coincides with the synchronizing code, causing the sequential selection of the extraction data instructed by the mode shifting portion to the pattern selecting portion to be changed to a sequential selection in which the kth extraction signal corresponding to the kth pattern is set as a candidate for the head word and the extraction data are selected starting from the kth extraction data.

The synchronization determining portion comprises a processing number generating portion capable of cyclically counting P integers as processing numbers in synchronization with output of the extraction signal, a second comparator portion for comparing the extraction signal with the synchronizing code, and a state determining portion for determining whether to make a transition between the synchronous state and the asynchronous state on the basis of the processing number and a result of the comparison in the second comparator portion."

As best understood, in Koyama, a shift register--with a number of buffers each having a storage capacity of m bits--is used to successively hold a second unit data that forms the input data signal. A pattern data extracting portion extracts L-bit-long data from the data held in the shift register in correspondence with first to K(≥1)th patterns in which the first unit data is sequentially assigned in the second data signal to obtain first to Kth extraction data. A first comparator portion compares each of the first to Kith extraction data with a synchronizing code as an indicator of a head word of the packet.

To the extent that Sakalian looks at consecutive bits positions to determine synchronization, Sakalian teaches away from using a shift register or pattern data extraction, as required by Koyama. Therefore, a skilled artisan applying the principles described in Sakalian is not motivated to use a shift register or perform pattern data extraction, in the manner described by Koyama, to determine synchronization. The requisite motivation to combine Sakalian with Koyama is lacking.

Furthermore, as best understood, it appears that combining Sakalain with Okayama will lead to an inoperable scheme for obtaining frame synchronization. Pattern data extraction, in the manner discussed in Koyama, appears incompatible with Sakalain's attempt to determine synchronization using bit positions. For example, Sakalian states:

"if five consecutively received bits in the selected framing bit position follow a predetermined pattern that the correct data bit position has been established" (Sakalian 1:42-45)

"If three out of five later received bits are detected as being incorrect, (after synchronization has been established) it may be assumed that the problem is not in the selection of the wrong framing bit position, but rather in the transmission medium. If any further data bits are received in the data bit position previously selected as the framing bit position, and these bits are received with incorrect values as compared to the predetermined pattern, it may be safely assumed that a new transmission medium needs to be established and resynchronization needs to be commenced from an initial set of values….." (Sakalian: 1:45-56)

Therefore, combining Sakalian with Koyama, in the manner suggested by the Examiner will yield an inoperable scheme for frame synchronization. Pattern data extraction, as shown in Koyama has no relevance or applicability to scheme used by Sakalian to determine synchronization.

Claim 1 is thus allowable over Kerns, in view of Sakalian, and further in view of Koyama. Claims 2-9 and 20 are dependent on claim 1 and are thus allowable for at least the same reasons as is claim 1.

Claims 10, 13-16 and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Taborek in view of Wright. Applicant respectfully traverse these rejections for at least the following reasons.

In rejecting claim 10, the Examiner asserts that Taborek teaches:

"counting mechanism for counting when the frame boundary is at the predetermined position in the data output (column 1, lines 13-31); a state machine, the state machine determining if the device is in a state of synchronization based on the counting mechanism".

Applicants respectfully traverses these assertions. There is no disclosure in column 1, lines 13-31 of Taborek of "a counting mechanism for counting when the frame boundary is at the predetermined position in the data output". In column 1, lines 13-31, Taborek states:

"A communication bus coupled between high performance devices, such as a communication bus providing for interconnection between integrated circuits (for "chip to chip" communication), Input/Output (I/O) devices, or between printed circuit boards via a connector, may need to operate at very high communication speeds. Moreover, interface logic and pin counts for implementing the bus may need to be minimized to reduce cost and complexity of the device in, or devices between, which the bus is located. Generally, a parallel bus will not meet the needs of many of today's applications due to being limited in operation to relatively slow data transmission speeds of one billion bits per second or less per parallel signal. A simple serial signal, although generally capable of operating at faster speeds than a parallel bus, will not meet today's needs as well, based at least in part on bandwidth demands. Applications today may require multiple serial signals operating in parallel to overcome these limitations. A parallel arrangement of serial signals is henceforth referred to as a "serial bus".

There is not even a mention of a "counting mechanism" in the above excerpts of Taborek. If the Examiner believes otherwise, he is requested to show with specificity, where in the above excerpt "a counting mechanism for counting when the frame boundary is at the predetermined position in the data output" is disclosed so as to provide Applicants with an opportunity to properly respond.

Contrary to the Examiner's assertions, Applicants also submit that there is no teaching or suggestion in column 5, lines 25-33 of Taborek of "a state machine, the state machine determining if the device is in a state of synchronization based on the counting mechanism."

Lines 25-33 of column 5 of Taborek is reproduced below:

"Note: hereinafter, an instance of a 10GBASE-X PCS function, state machine, or process, described in IEEE Draft P802.3ae specification, Clause 48, as embodied in the XGXS described in IEEE Draft P802.3ae specification, Clause 47, may be referred to simply as "the

PCS function", "the PCS state machine", or "the PCS process". Furthermore, references to Clauses 47 and 48 of the IEEE Draft P802.3ae specification may be referred to simply as "Clause 47" and "Clause 48""

There is no description whatsoever, in the above excerpt however of "a state machine, the state machine determining if the device is in a state of synchronization based on the counting mechanism", as required by claim 10. Furthermore, since Taborek fails to disclose a "Counting mechanism", Taborek also fails disclose a state machine that can determine synchronization "based on the counting mechanism", as required by claim 10. Taborek, whether taken alone or in combination with Wright fails to teach or suggest claim 10. Claim 10 and its dependent claims 11-17 are thus allowable.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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